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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,327	01/22/2004	Arkadiy Peker	PDS-015	2698

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MICROSEMI CORP - AMSG LTD.
C/O LANDONIP, INC
1700 DIAGONAL ROAD, SUITE 450
ALEXANDRIA, VA 22202-3709

EXAMINER	
PARRIES, DRU M	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
07/16/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Skahn@microsemi.com

Office Action Summary	Application No.	Applicant(s)	
	10/761,327	PEKER ET AL.	
	Examiner	Art Unit	
	DRU M. PARRIES	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9-43 and 46-50* is/are rejected.

7)☒ Claim(s) *44 and 45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5-12-08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-6, 9-16, 18-37, 39, 43, and 46-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Yoneda (2003/0218384), and Kawabata et al. (4,677,535). Regarding independent claims 1, 27, 43, and 48, and dependent claims 2, 3, 9, 20, 35, and 49-50, APA teaches a LAN comprising a powered device (80), a hub (30) with a controller (20), and communication cabling (60) connecting the powered device to the hub comprising first (the middle two pairs) and second (the top and bottom pairs) sets of twisted wire

pairs carrying power and/or data. APA also teaches a first DC power source (40) being associated with midspan power insertion equipment (160) adapted to supply and return power over the first set of wires. APA also teaches a second set of twisted wires (top and bottom of Fig. 1c) communicating data. APA fails to explicitly teach a second power source, a combiner that combines the received first and second power source outputs and outputs a high power output. Yoneda teaches a power control method comprising combiner circuitry operative to receive a first power (via wire 5) and a second power (via wire 6) and to combine the currents of the two powers to a combined high power output and to maintain a near even balance between the currents of the received first and second powers by a current share circuit, which is implemented into the controller. Yoneda also teaches a control circuit for sensing the successful operation of the combiner by sensing the combined high power signal (via each individual output current) and supply the combined high power signal to a powered device in response to the sensed successful combined high power signal operation. (Fig. 1; [0003], [0011], [0031]-[0034], [0048]-[0051]) Yoneda fails to explicitly teach a second DC power source, however, Kawabata teaches a power control system with plural parallel converters outputting to a single load, wherein each converter has its own corresponding DC power source (Fig. 1). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement another DC power source, in parallel with the first power source of APA, having its own set of wire pairs into APA's invention to allow for more available power to the system, and in case the first power source fails the system doesn't have to shut down. It also would have been obvious to one of ordinary skill in the art at the time of the invention to implement Yoneda's combiner circuitry

into the load side of APA's invention to be able to have the ability/choice to supply twice as much current to a load, if necessary.

Regarding claims 4, 10, 12, 14-16, 23, 30, and 31, APA, Yoneda, and Kawabata fail to explicitly teach the location(s) of the first and second power sources and the combiner in APA's invention. It would have been obvious to one of ordinary skill in the art at the time of the invention to have the first and/or second power source associated with the hub and/or the midspan power insertion equipment and to have the combiner inside or outside of the powered device/load, since it has been held that rearranging parts of an invention involves only routine skill in the art. *In re Japikse*, 86 USPQ 70.

Regarding claims 5 and 6, one could say that the first and second power sources are simultaneously isolated and not isolated from each other. They are isolated initially from each other at their outputs, and then once the combiner combines their signals, one could say they are not isolated from each other at that point.

Regarding claims 11, 13, 21, 28, none of the references explicitly teach the elements of the LAN system conforming to the IEEE 802.3af-2003 standard, however, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the elements of APA's LAN system conform to the above IEEE standard so that the system will function safely and in correlation with most systems around the world and therefore could easily be implemented into another system.

Regarding claims 18, 19, 46 and 47, Yoneda teaches Yoneda teaches the combiner circuitry to transmit a signal to the first or second power source(s) (via converters 1, 2) indicating

that the combiner is operative to produce said high power output (Fig. 9, C2-C5). The signal also comprises a change in the class identification (i.e. "intermittent" to "continuous").

Regarding claims 22, 24-26, 29, and 32-34, APA fails to explicitly teach what the powered device (PD) is. Yoneda teaches the load in his circuit being a laptop computer ([0003]). He also teaches his load operative in a low and high power mode responsive to the combiner, which is operable to supply low power to said load for operation in said low power mode in the absence of the combined high power. The signal to the load of the low power supply operation is the power level output to the load.

Regarding claims 36, 37, and 39, Yoneda teaches his combiner circuit comprising a first DC/DC converter (1) associated with the first power input and a second DC/DC converter (2) associated with the second power input, which are connected in parallel.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Yoneda (2003/0218384), and Kawabata et al. (4,677,535) as applied to claim 1 above, and further in view of Parsi et al. (6,856,629). APA, Yoneda, and Kawabata teach an electrical system as described above. They fail to explicitly teach the hub operating according to 10 Base-T. Parsi teaches a network comprising a hub operating according to 10 Base-T (bottom of Col. 6, top of Col. 7). It would have been obvious to one of ordinary skill in the art at the time of the invention to have the hub operate according to 10 Base-T since APA was silent as to the operation of the hub and Parsi teaches a method of operation known in the art to work.

6. Claims 38 and 40-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Yoneda (2003/0218384), and Kawabata et al. (4,677,535) as applied to claims 27 and 37 above, and further in view of Larner (4,028,559). APA, Yoneda, and

Kawabata teach an electrical system as described above. They fail to explicitly teach the combiner having the converters comprising two primary windings and one secondary winding. Larner teaches a combiner comprising a transformer (T) having a first primary (b-a; part of the first DC-DC converter) associated with a first power source (VZ1), a second primary (b'-c; part of the second DC-DC converter) associated with a second power source (VZ2), and a secondary (d-e; part of both DC-DC converters) associated with a combined higher power. Therefore, one could say the first and second DC-DC converters are in series (on the secondary side) and in parallel (on the primary side). Larner also teaches a PWM controller (for SW1&SW2) associated with both the first and second DC-DC converters. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement Larner's combiner circuitry into the combiner of the modified APA invention since Larner teaches a configuration that is known in the art and would allow for a wider range of outputs from the combiner.

Allowable Subject Matter

7. Claims 44 and 45 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dru M. Parries whose telephone number is (571) 272-8542. The examiner can normally be reached on Monday -Thursday from 9:00am to 6:00pm. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry, can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMP

7-9-2008

/Stephen W Jackson/

Primary Examiner, Art Unit 2836